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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/603,132	06/23/2000	Brian A. Vaartstra	150.00650102	3538

7590 07/26/2005

Mueting Raasch & Gerbhardt PA
PO Box 581415
Minneapolis, MN 55458

EXAMINER	
LEE, EUGENE	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/603,132	VAARTSTRA ET AL.
	Examiner	Art Unit
	Eugene Lee	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *45-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *45-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/9/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/12/05 has been entered.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the opening has an aspect ratio greater than about 3 (claims 60, and 66) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 69 thru 74 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not describe the surface defining the opening being not a silicon containing surface.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 45 thru 48, and 54 thru 59 are rejected under 35 U.S.C. 102(b) as being anticipated by Komatsu 5,907,789. Komatsu discloses (see, for example, FIG. 7C) a semiconductor device comprising a silicon semiconductor substrate (substrate assembly) 70, and metal silicide layer (diffusion barrier layer) 120. In column 22, lines 29-44, Komatsu discloses the metal silicide layer may be made of ruthenium. Komatsu also discloses that various methods can be used to form the metal silicide such as physical vapor-phase growth method or chemical vapor-phase growth method.

Regarding claims 46, and 47, see, for example, column 5, lines 56-65, wherein Komatsu discloses that x may be 2.

Regarding claim 48, see, for example, column TiN layer (one or more additional conductive layers) 114.

Regarding claim 54, see, for example, FIG. 7C wherein Komatsu discloses a MOSFET (active device) 105 and metallization material (interconnect) 118.

Regarding claim 56, see, for example, FIG. 7C wherein Komatsu discloses a TiN layer (conductive contact material) 114.

7. Claims 45 thru 48, 50, and 51 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsubara et al. 5,122,923. Matsubara discloses (see, for example, Fig. 1) a capacitor (semiconductor device structure) comprising a silicon substrate (substrate assembly including a surface) 1 and a lower electrode (diffusion barrier layer) 3. In column 4, lines 24-27, Matsubara

discloses the lower electrode being made of layers of ruthenium, ruthenium oxide, ruthenium silicide and stacked structures.

Regarding claim 48, see aluminum electrode (one or more additional conductive layers) 5.

Regarding claims 50 and 51, Matsubara discloses (see, for example, Fig. 1 and column 3, lines 43-47) a capacitor structure comprising a lower electrode (first electrode) 3, dielectric layer (high dielectric material) 4, and upper electrode (second electrode) 5.

8. Claims 45, 46, 50, and 51 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuroiwa et al. 6,239,460 B1. Kuroiwa discloses (see, for example, Fig. 10 and column 13, lines 12-14) a semiconductor device structure comprising a substrate (substrate assembly) 101 and a ruthenium silicide layer (diffusion barrier layer) 132.

Regarding claims 50 and 51, Kuroiwa discloses (see, for example, FIG. 10) a capacitor structure comprising a metal electrode (first electrode) 130/132, capacitor dielectric 115 and upper electrode (second electrode) 116. In column 13, lines 11-15, Kuroiwa discloses the ruthenium silicide layer 132 is formed from a portion of metal electrode 130.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 48, 49, 54 thru 59, 61 thru 65, and 67 thru 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroiwa et al. '460 B1 as applied to claims 45, 46, 50, and 51 above, and further in view of Lee et al. 5,872,041. Kuroiwa does not disclose a silicon containing region. However, it was well known in the art to use a substrate made of silicon (silicon containing region). Lee discloses (see, for example, column 2, lines 23-29) a semiconductor device on a silicon substrate 300. It would have been obvious to one of ordinary skill in the art at the time of invention to use a silicon containing region in order to form a semiconductor device and have diffused regions formed therein since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claims 48 and 49, see FIG. 10 wherein Kuroiwa discloses a metal electrode (one or more additional conductive layers) 130 and column 9, lines 39-42 wherein Kuroiwa discloses the metal electrode comprising ruthenium (Ru) or iridium (Ir).

Regarding claim 54, Kuroiwa discloses (see, for example, FIG. 10) a DRAM (integrated circuit structure) comprising a substrate assembly including a substrate (silicon containing region) 101, transfer gate transistor (active device) 103b, and a plug (interconnect) 111 including a ruthenium silicide layer 132.

Regarding claim 56, Kuroiwa discloses a metal electrode (conductive contact material) 130.

Regarding claims 58, 59, 61, 62, 64, 65, 67, and 68, Kuroiwa discloses the ruthenium silicide layer (conformal layer) 132 within an opening of the insulating film 110. The aspect ratio (ratio of height to width) is clearly greater than 1.

Regarding claim 63, Kuroiwa discloses (see, for example, FIG. 10) a capacitor comprising a metal electrode (first electrode) 130, capacitor dielectric film (high dielectric material) 115, upper electrode (second electrode) 116, and ruthenium silicide layer (diffusion barrier layer) 132.

Regarding claim 69, Lee discloses (see, for example, column 2, lines 23-29) the substrate may be germanium or gallium-arsenide.

11. Claims 52 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroiwa et al. '460 B1 in view of Lee et al. '041 as applied to claims 48, 49, 54-59, 61-65, and 67-74 above, and further in view of Matsubara et al. 5,122,923. Kuroiwa in view of Lee does not disclose the first electrode comprising one or more additional conductive layers. However, it was well known in the art at the time of invention to use multiple layers in the electrodes of a capacitor. In column 4, lines 25-27, Matsubara discloses a lower electrode comprising multiple layers of ruthenium, ruthenium oxide, ruthenium silicde and stacked structures consisting of these materials. It would have been obvious to one of ordinary skill in the art at the time of invention to have the first electrode comprising one or more additional conductive layers in order to form an adequate bottom electrode, and since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis paper Co. vs. Bemis Co., 193 USPQ 8.

12. Claims 60, and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroiwa et al. '460 B1 in view of Lee et al. '041 as applied to claims 48, 49, 54-59, 61-65, and

67-74 above, and further in view of Lee 5,897,350. Kuroiwa in view of Lee '041 does not disclose the opening having an aspect ratio greater than about 3. However, Lee '350 discloses (see, for example, FIG. 4B) a semiconductor device comprising a contact hole (opening) 32 having an aspect ratio greater than 3. It would have been obvious to one of ordinary skill in the art at the time of invention to have the opening have an aspect ratio greater than about 3 in order to provide higher integration in a semiconductor device since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Product-by-Process Limitations

13. While not objectionable, the Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or *otherwise*. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

The limitation "chemical vapor codeposited" merely recites a method of forming and does not deviate from the **structure of a diffusion barrier made of $RuSi_x$**.

Response to Arguments

14. Applicant's arguments with respect to claims 45-74 have been considered but are moot in view of the new ground(s) of rejection.

On page 8, paragraph 4 of the applicant's argument filed 5/9/05, the appellant argues that the diffusion barrier layer made by a method of "chemical vapor codeposition" is different than the layer made by a method of "sputtering". However, the claims, as presented in the instant application, do not state any of these structural differences. The claims only state a diffusion barrier made by a method of chemical vapor deposition and do not state at all any structural limitations that may or may not be attributed to this method. Also, Komatsu 5,907,789 and Agostinelli et al. 5,017,551 respectively disclose (see, for example, column 22, lines 29-44 of Komatsu and column 20, lines 11-16 of Agostinelli) the two methods as interchangeable in forming the structure of a ruthenium silicide layer.

On page 9, paragraph 1, the appellant refers to "Declaration Under 37 C.F.R. 1.132" (filed 1/27/03) that states structural differences between a sputter coating diffusion barrier layer and a chemical vapor deposited diffusion barrier layer because the underlying substrate to a sputter coated diffusion barrier layer, not the diffusion barrier layer itself, may have surface damage. However, these statements in the Declaration are conclusionary in nature and not absolute. The greater likelihood that the underlying substrate of a sputtered barrier layer as opposed to a chemical vapor deposited diffusion barrier layer does not clearly suggest that the

structure of the semiconductor device with a sputtered barrier layer will be always be different than a semiconductor device with a chemical vapor deposited diffusion layer. The claims do not state any structural differences because of these methods.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
July 14, 2005